IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 13, Issue 2, Ver. II (Mar. - Apr. 2018), PP 89-96
www.iosrjournals.org

Design and Verification of Five Port Router Network

Avinash G[1], Megha N[2]
[1](Electronics and Communication Engineering, Sahyadri College of Engineering and Management, India)
[2](Electronics and Communication Engineering, Sahyadri College of Engineering and Management, India)
Corresponding Author: Avinash G

Abstract: *A Network-on-chip (NoC) is a new technique in complex system-on-chip (SoC) designs which helps to facilitate efficient on chip communication among networks. It permits decoupling of communication, computation and also permits scalable communication. Information is transmitted in the form of packets through networks. Routers help to route the data. So efficiency of router required to be more with higher throughput and lower latency. The proposed methodology incudes design, analyze and implementation of router architecture for NoC communication. Routers consists of five ports in which four are connected in different directions to other ports and processing element is connected to fifth with the help of network interface. The first architecture consists of basic router together with scheduler and demultiplexer. The second architecture includes arbiter and crossbar switch. The third architecture is developed with help of CDMA technology which is popular in wireless communication. By comparing three architectures the performance in terms of latency, throughput and delay, performance of CDMA router is much efficient then rest of two.*

Date of Submission: 16-04-2018 Date of acceptance: 04-05-2018

I. Introduction

Biggest challenge for the IC designers is to accommodate a billion numbers of transistors, millions of gates and many numbers of circuits as well as designs in a single integrated circuit (IC). All these problems have overcome by the most fruitful designers of integrated circuit to provide efficient operation and correct functionality of the integrated circuit. The major area of interest in the design of integrated circuit is the price affectivity when there is increase in integration. Cost reduction is important aspect of integrated electronics. Advantage in the price increase continues with the technological evolution towards functions of huge number of circuit production on a substrate of single semiconductor. A constant pace is kept with such type of intricate steps of integration that the design engineers have developed new design technique called System-on-Chip (SoC). It consists less space in which maximum technology is implemented. The SoC design is impacted more by the property which is called as intellectual property (IP) core. Core of an integrated circuit is a predesigned and preverified block of silicon circuit. Usually core contains gates which are at least 5,000 in number and uses of these are in applications with more complexity and large semiconductor chips. Examples of cores areprocessors, memory controllers, or peripheral devices which are PCI bus controllers or MAC Ethernet. The property IP core is related to the entire single vendor which belongs to semiconductor industry. IP cores are the building blocks of most of the systems on chip designs for implementing complicating and large applications of embedded systems. The system on chip includes hardware's like processors, controllers, digital signal processors,memories peripherals and software's take control of hardware's and various custom logic blocks.

II. Overview of No

This chapter presents an overview of Network-on-Chip (NoC) and its parameters. Books and research papers are present which contains theories, concepts and definitions of micro networks. Here we present relevant concept and theories which holds good for NoC systems.

NoC Building Blocks

NoC allows IP cores to interact with an on-chip network. Figure 3.1 shows Illustration of Four Basic NoC Building Blocks, which has of four basic functional blocks. These blocks contain routing node, IP cores, the links and network adaptor. IP cores are not a part of design but are particular for the application.

NoC Parameters

To enhance NoC performance, the NoC parameters are chosen depending on the particular application. The general network design purpose is to avail maximum designer flexibility. Most of the network parameters dependent on other parameters and few can be created flexibly. The selection of parameters can be done based

on testing and evaluation. Network parameters are divided into three groups that are Infrastructure, Communication Mechanism, and Mapping.

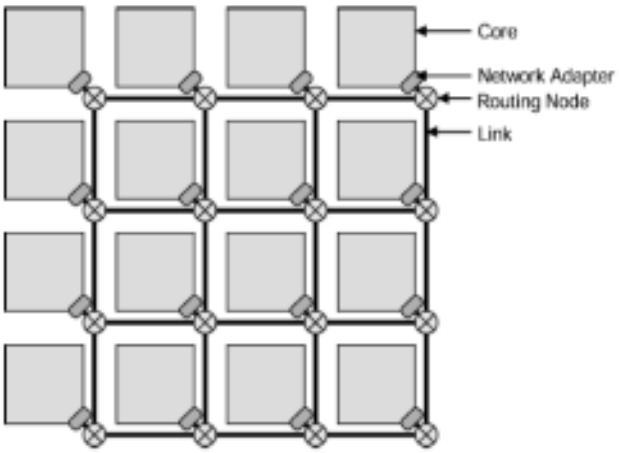

Fig. 1 Illustration of Four Basic NoC Building Blocks

Router

The major essential part in network on-chip is router. The router is backbone of network on-chip system. So it is necessary to design in such a way that efficiency is high and throughput is large. In order to direct the traffic from a source point to destination point router is essential. The flow of data is coordinated by router which is very much essential in communication network.

There are basically three ports in the router namely input, output and local port. The input port is connected to the output port by switching matrix. Local port is used to connect the router to the respective Ip core. Router behaves as brilliant device which accepts the input data packet, finds out the destination of the input and decides the best path for the movement of data all the way from source side to destination side. The architecture of router decides the delay of the critical path that affects per-hop-delay as well as latency of network. Because of this the router should be designed in such a way that latency which is required is met as well as throughput requirement and constraints in power.

The network performance is decided by the router design efficiency. The information carried by the incoming signal is decoded by router which is dependent on the function of routing and the destination to which the information is transferred. The building of the router is done based on the OSI model of network on-chip. The individual layer has separate function to perform.

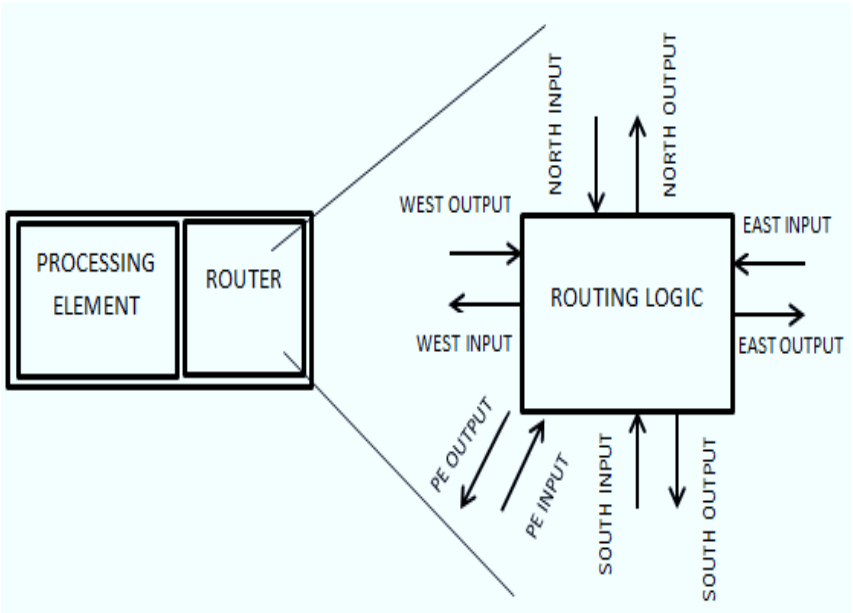

Fig. 2 A typical routing node

Network topology

Topology of the on-chip network determines the physical-layout and also connection between channel and nodes in network. The number of routers to which the message should travel is determined by the topology and also length of interconnection between the routers. The pass over routers and links incur energy, the router count is also affected by topology which also effects the consumption of network energy.

Moving on sum total numbers of alternative paths in between the nodes is decided by the topology, by affecting how good network can handle traffic and provides the support for bandwidth requirement. The main area at which the designers are required to work during building of on-chip network is the topology which has to be used.

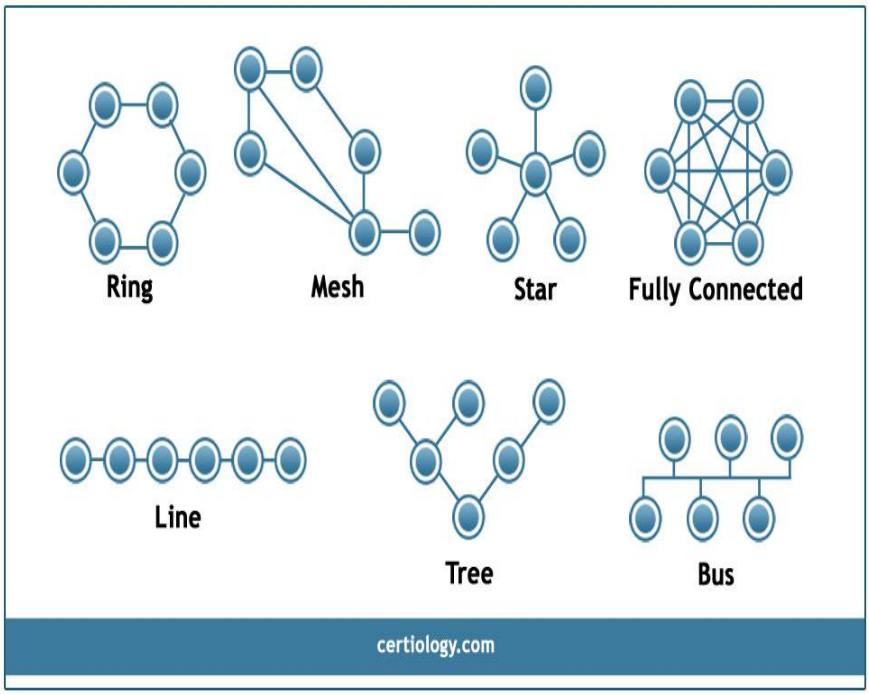

Fig. 3 Different types of network topologies

Mesh

The layout topology efficiency of the mesh topology is very much impressive and because of this it is adopted by many research groups. In a simple way it can indicate the resources of on-chip and also electrical property of the topology is very good. The network which is of mesh type contains n-rowsandm-columns. The router is placed at point of intersection between the two wires and computational resources are placed near the router. In this topology resource of the router and address of the router is represented in x-y coordinates. Mesh shaped network contains M column and N row. The disconnection among network may not create big problem.

Torus

The updated version of basic mesh-network is known as torus network. The torus-network is also mesh at which head of the column is connected to tail of column and right side of the row is connected to left side of row. The diversity in the path of torus is better compared to mesh and the numbers of routes are also less in number.

Tree

The nodes behave as router and leaves behave as computation resource in case of tree topology. The routers which are above leaves are referred as leaf's ancestors and respectively the leaf below the ancestors are referred as children. In this there are many separate routes between each node. The failure at one point may cause problem to remaining networks.

Butterfly

This network is either uni-directional or bi-directional and has a shape of butterfly. Also it uses a particular routing. Information is arrived in the packet form to input port at left portion of network and is directed to right output on the right portion of network.

Polygon

In this type of network the data which travels in the form of packet in a loop from one router to another. Polygon network is in the form of circular network. When the chords are added together to circle the network will become diverse. The topology is named as spidergon when there are only chords in-between opposite router.

Star

This consists of central network at the centre of star and sub network in the star spikes. The central router carries handles the data flow between the spikes. Hence the capacity of central router should be large enough to support data flow. This increases the possibility of being congested central network. Error in one point of network doesn't create problem to rest of the connections.

III. Proposed Methodology

The 2-d mesh topology is most common due to its regular structure and grid type shapes which are appropriate for chips of two dimensional layouts. In mesh topology distance between all nodes equal so it is easy to implement. During routing process addressing of cores becomes simple. The network size is independent on local interconnection between routers and resources. In 2-D Mesh routing is easy which result in short clock cycle, potentially small switches, overall scalability and high capacity. Therefore mesh topology is preferred. Mesh topology consists of 4 inputs and 4 outputs from or to other routers. It has another input and output from or to the PE. Router is designed for the mesh topology implementation.

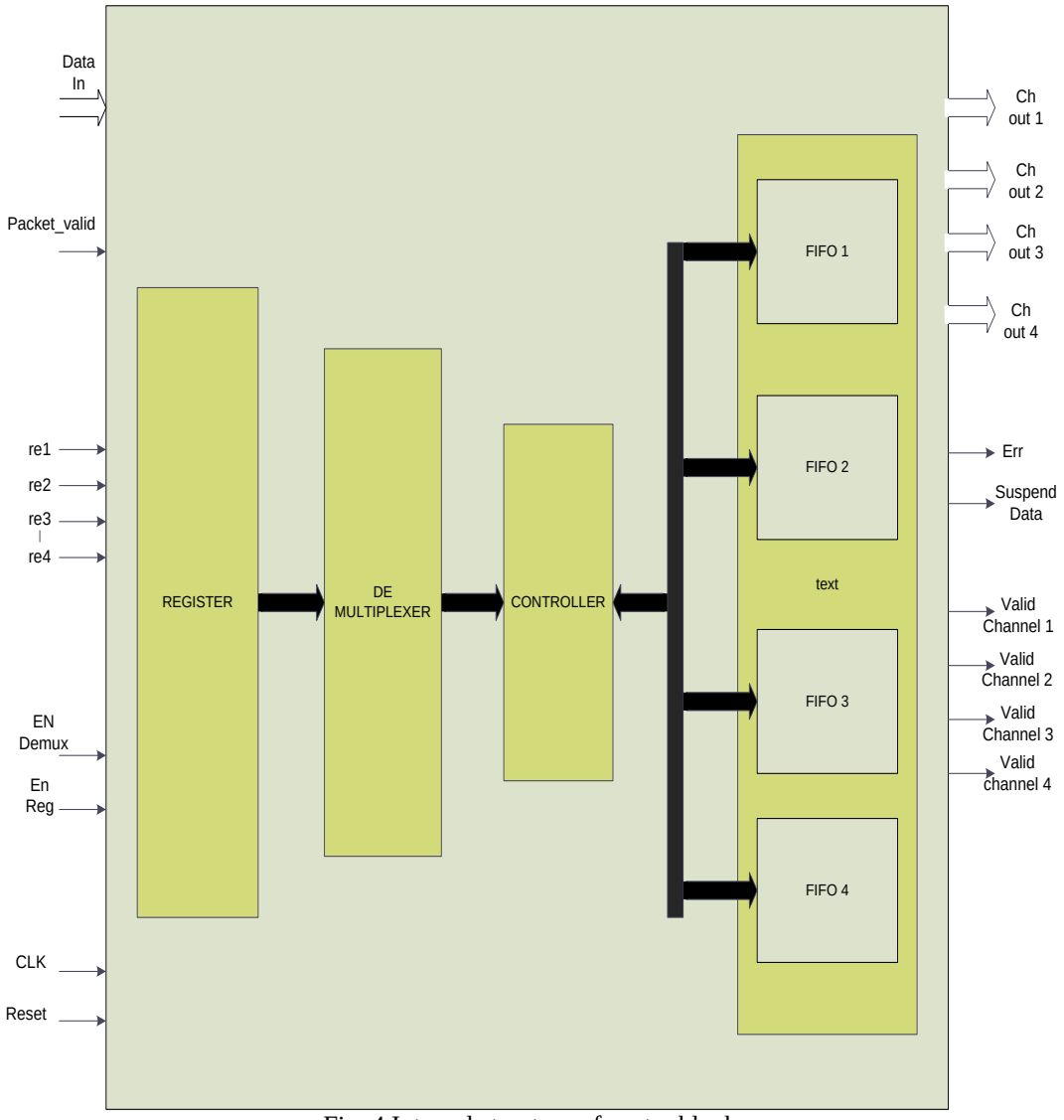

Fig. 4 Internal structure of router block

In proposed router architecture contains four blocks that are FIFO, register, controller and demultiplexer. The purpose of register is same as the buffer in which input content is stored. The channel is provided by demultiplexer that sends the input content to the particular output port. The write and read operations are managed by FIFO which is a first in first out memory queue with control logic. The flow of data can be controlled between source and destination by using it. The performance of router is increased by using FSM deterministic routing. Here five port network routers are designed. In packet form router accepts the data which consist of three parts. They are frame check sequence, header and data. The width of packet is 8 bits and the length lies between 1 to 63 bytes. Based on packets destination address the router sends the packet to respective ports. Figure4 shows the router blocks block diagram. It consist of has five inputs and five output ports which are used to design the central router of Mesh topology which is shown in Figure 5 Using round robin mode data is transferred to all outputs from inputs by this block.

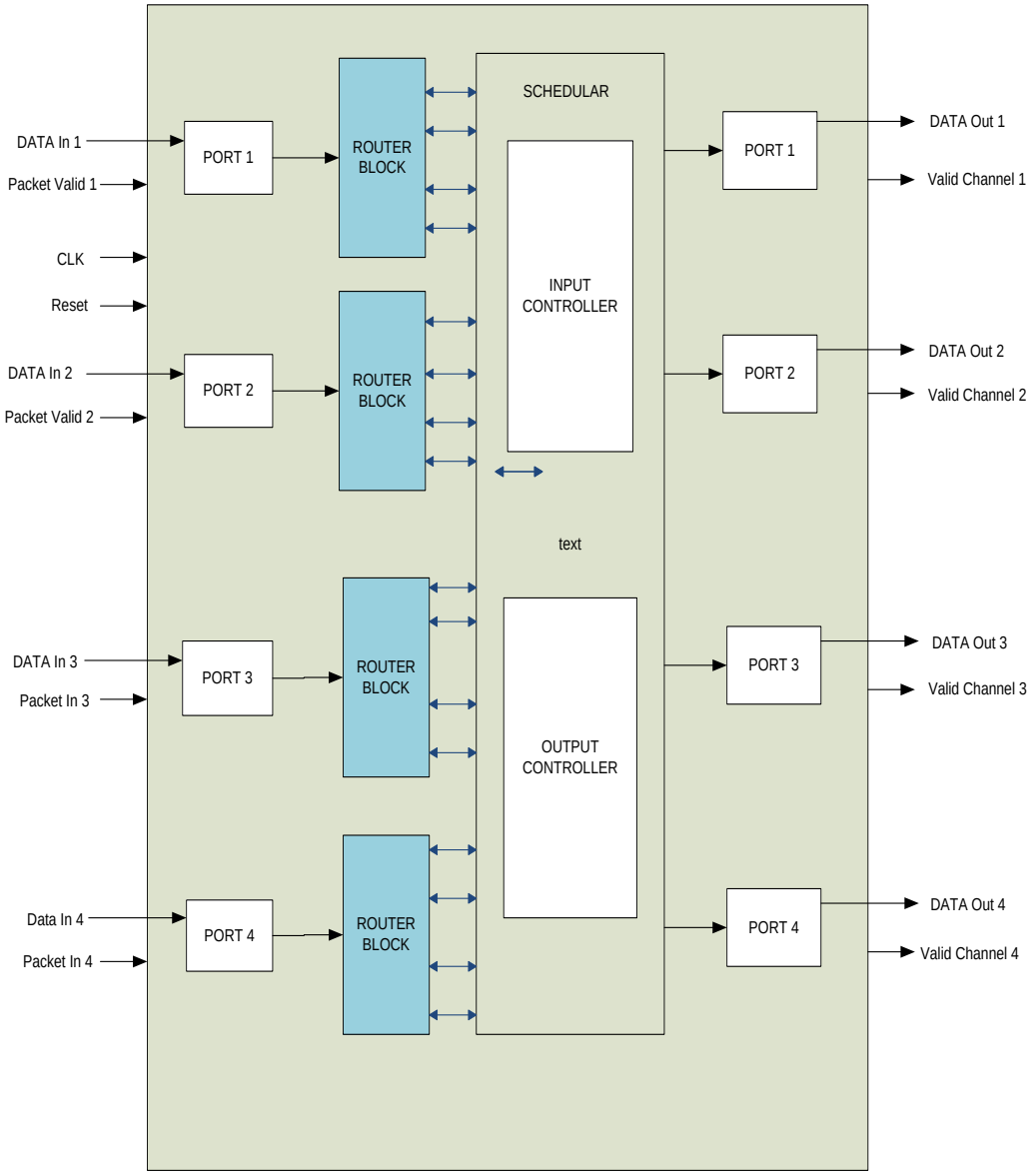

Fig. 5Internal structure of mesh router

Resister

The 8 bit register is designed which consist of enable, clock and register. The output is obtained only when clock is posedge and enable is high and reset is low. The register keeps current value when enable remains low. The demultiplexer input is taken from output of register. Here register behaves as a buffer and temporally values are stored. As the register is designed here, it first stores the input data and when all the conditions are satisfied it is forwarded. To avoid congestion forward flow control and store is used.

Demultiplexer

Here 1:4 bit demultiplexer is designed to define the four output ports. The select signal is indicated by last two bits of the input data and it indicates the port. Table I shows the output port tells about last 2 bits. Demultiplexer is used to transmit the data which is going to particular output port from register block. The demultiplexer contains an enable pin. When enable pin is high demultiplexer directs the data to the appropriate output port. Other write enable pin and output ports should remain zero. The individual FIFO unit is connected to output of the each port.

FIFO

The designed FIFO block consists of 8 bit width and stores data in memory array of 0 to 15 which is known as depth of memory array. The data coming from individual ports are stored in are four fifo's and it performs the write and read operations. FIFO consists of two control signals that are fifo_empty and fifo_full. The multi-bit data passed from 1 clock position to another using FIFO or flow of data is controlled between source side and destination side. Write and read operations are performed with help of synchronous clock. Synchronous clock is used for both write and read operation. When reset is low and posedge of clock write operation is performed, write enable pin is high and fifo is not full.

The data is written in to FIFO memory in these conditions. At rising edge of clock read operation is performed and read enable pin also becomes one. The data is read operation is performed from FIFO memory when FIFO is not empty. When fifo_ full signal is one, it indicates that FIFO is written with all locations present and it is not possible write further data inside it. Similarly when fifo_empty signal is one, it indicates that inside FIFO all locations are empty and it is not possible to read data from FIFO memory. There are four fifo blocks with four fifo_empty signals and fifo_full signals are input to the FSM controller.

FSM Controller

The control signals are generated by this module when new packets reach to router. Other modules use these control signals to send data to the output. As controller is connected to output of demultiplexer, each ports data is received by controller when the port enable pin is one as well as packet_valid signal is one of respective ports. The data is accepted only when reset is low a posedge of clock. The controller will handle both fifo_empty and fifo_full signals.

There are four FIFO output ports. The controller stars checking which FIFO is empty and which FIFO is full and write data according to port address to respective FIFO when controller pin is high. The data read is performed when fifo_full is one and send it to the respective controller's output port. The data becomes ready to transmit when read task is completed. It is indicated by the respective valid channel signal when it becomes high.

The controller consists of four output ports with four valid channels. The channel becomes busy in communicating when any one of the channel is low, and respective fifo_empty signal is one. It means that data is ready to be written into the present fifo. When the suspend_data signal becomes low, router is ready to take new data from the input and latched data is sent to the FIFO. The data is written in to present FIFO when we pin is generated. The FSM logic is used in present controller, due to this cycle for each output port is repeated and hence it increases performance.

IV. RESULT

The simulation of the proposed system is done with the help of Xilinx. It consists of mainly router module which has different sub modules that are Multiplexers, arbiter (controller), FIFO and router. The controller consists of single input port and 4 output ports. RTL schematic and behavioral model of these sub modules are obtained. Combining all these sub modules, final simulation output and RTL schematic of five port router network is obtained.

Figure 6 shows router block RTL model and figure 7 shows router behavioral model. Data input, packet_valid, clock and reset is given as input to router block. There are four router blocks in mesh router. The output of router is given as input to scheduler.Figure 7shows the simulation output of the router block which includes single input port and 5 output ports. When reset is zero and clock is at posedge router block takes the input data. Because of this suspend_data signal goes low and EN_REG, re pin as well as EN_DEMUX pin goes high. When input bits are 10011000 it indicates the data should be available at port I. when FIFO becomes full, controller starts to send signal and data is obtained at ch_outl. When the valid channel becomes high the data at ch_out1 is ready to transmit.

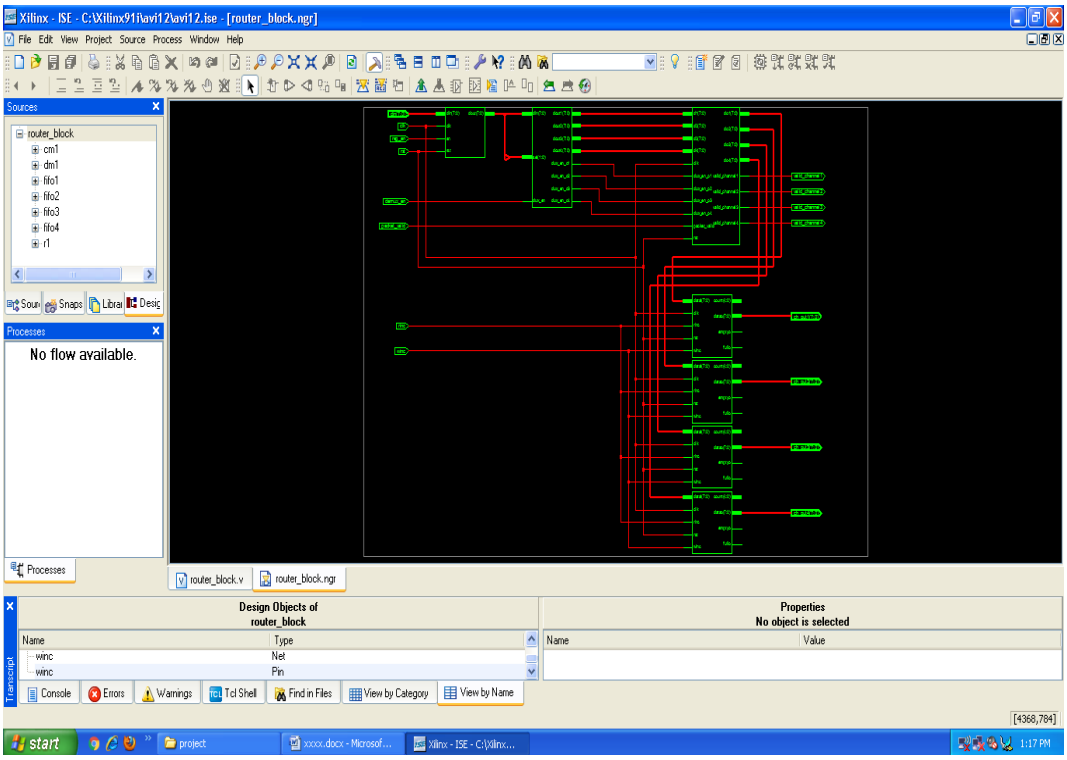

Fig. 6 Router Block RTL model

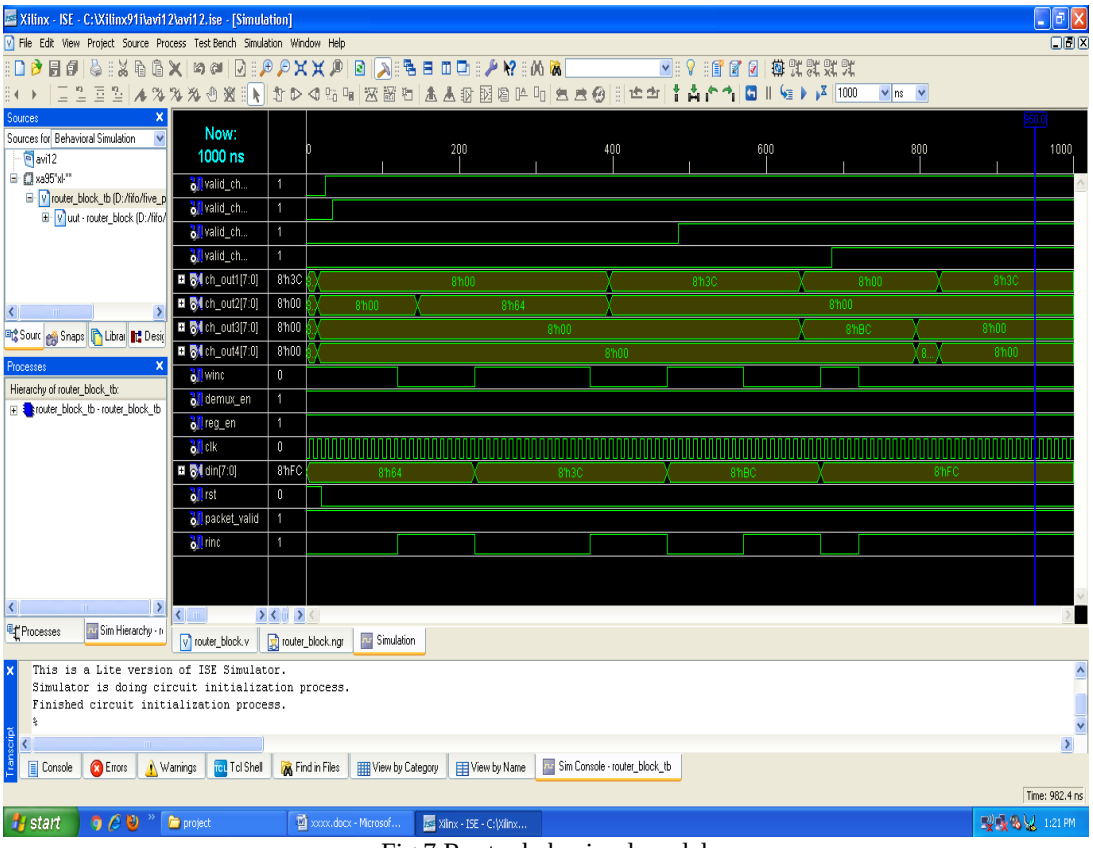

Fig.7 Router behavioral model

V. Conclusion

As the design complexity increases, designers have to concentrate on communication aspect. With adopting NoC for future SoC systems we can resolve the issues of communication. Leading to higher performance at reasonable area and costs, NoCs are solution for concurrent transactions among IP cores. NoCs

support reusable architecture; we can again concentrate on the computation aspect. NoC with its flexible design gives much more potential than it's previous. Recent modifications in NoC designs with standard architecture have to be evaluated and more research has to be done in this area in feature to improve its performance.As research progressed, some interesting matters are added during router development time of NoC. Due to lack of time these are not considered in research but these can be used for further NoC improvement in feature.

References

[1] Shubha B C, Srinkanta P, "FPGA Implementation of Network on Chip Framework using HDL", Students' Technology Symposium(TechSym), IEEE PP. 151-155, April 2010.

[2] Swapna S, AyasKanta Swain, Kamala KantaMahapatra,"Design And Analysis of Five Port Router For Network On Chip", Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics(PrimeAsia)20 12.

[3] HaythmElrniligi, Ahmed A. Morgan, M. Watheq EI-Kharashi, and Fayez Gebali "Performance Analysis of Networks-on-Chip Routers", Department of Electrical and Computer Engineering University of Victoria, BC, Canada V8W 3P6 Mentor Graphics Egypt, Cairo I 134I, Egypt, IEEE-2007

[4] MajdiElhajji, BrahimAttia, AbdelkrimZitouni, RachedTourki,Jean-lucDekeyser, "FERONOC:Flexible and Extensible Router Implementation For Diagonal Mesh Topology" Author manuscript, published in Conference on Design and Architecture for Signal and Image Processing(20 II).

[5] M.S.Suraj, D.Muralidharan, K. Seshu Kumar, "A HDL Based Reduced Area NoC Router Architecture"978-1-4673-5301-4/\3/$31.00 © 20\3 IEEE.

[6] Angelo KutiLusala, Philippe Manet, Bertrand Rousseau, Jean-Didier Legat "NOC IMPLEMENT A nON IN FPGA USING TORUS TOPOLOGY" International Conference on Field Programmable Logic and Applications, PP 778-781, IEEE-2007.

[7] PratikshaGehlot, Shailesh Singh Chouhan, "Performance Evaluation Of Network on Chip Architectures",Departrnent of Electronics andcommunication Institute of Engineering & Technology DA VV Indore, India, International Conference on Emerging Trends in Electronics and Photonic Devices & Systems (ELECTRO-2009).

[8] Fernando Moraeset.a! A Low Area Overhead Packet-switched Network on Chip: Architectutre and Prototyping. In IFIP VLSISOC 2003, pages 318-323, 2003.

[9] Theodore Marescauxet.a! Interconnection Networks Enable Fine-Grain Dynamic Multi-Tasking on FPGAs. In FPL' 2002, pages 795-805, September 2002.

IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) is UGC approved Journal with Sl. No. 5016, Journal no. 49082.

Avinash G "Design and Verification of Five Port Router Network." IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) 13.2 (2018): 89-96.